Controlling **Lea**kage power in NanoCMOS SoCs
FP6-2004-IST-4-026980-IP-CLEAN

Leakage Aware Design of Nanometer CMOS Circuits

One-day intensive course
29 March, 2007, Budapest, Hungary
Budapest University of Technology and Economics, Department of Electronics Technology

This course is the fourth one in a series of "Leakage Aware Design for Next Generation's SoCs" courses and workshops in Europe. The course will have a strong focus on the physics and modeling of leakage currents, foundations of leakage control and estimation, as well as, practical design aspects and optimization to design the next generation of low-power nanometer CMOS circuits.

The series of "Leakage Aware Design for Next Generation's SoCs" courses and workshops is developed by the European CLEAN project, in order to make its all achieved R&D results available to the scientific and industrial communities during and after project lifetime.

This course is addressed to designers of CMOS digital circuits as well as researchers, academic teachers and Ph.D. students. If you know someone who might be interested in the course, please bring it to her/his attention. For more information, please consult www.ett.bme.hu/clean-minos/.

Course Program	**29 March, 2007**	**BME, Budapest, Hungary**
Registration		10:30 - 12:30
Lunch		12:00 - 12:30
M1 Introduction, state of the art, roadmap, and Leakage power models	Prof. Wieslaw Kuzmicz WUT, Warsaw, Poland	12:30 - 14:30
Short coffee break		14:30 - 14:45
M2 Techniques to control leakage power at technology and device level	Edith Beigne CEA-LETI, France	14:45 - 15:45
Coffee break & refreshments		15:45 - 16:15
M3 High level leakage estimation and optimization	Dr. Domenik Helms OFFIS, Oldenburg, Germany	16:15 - 18:15
Short coffee break		18:15 - 18:30
M4 Informal Discussion, Hot topics, and Interactive Q&A	All presenters + participants	18:30 - 19:30
Break		19:30 - 20:00
Networking Dinner		20:00 - 22:00

No registration fee	***Registration deadline: 27th Feb, 2007***

After registration: participation in all sessions and in the MINOS workshop, one copy of printed materials, all meals and coffee breaks from lunch on 29th March to lunch on 30th March, 2007. The registration fees of reasonable number of delegates of MINOS Partners are covered by the MINOS network.

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MINOS Information-day
Micro- and Nano-System Developments and Applications

Lunch-to-lunch workshop
29-30 March, 2007, Budapest, Hungary
Budapest University of Technology and Economics, Department of Electronics Technology

The Leakage Aware Design course will be organized in collaboration with the MINOS-EURONET Project, in the frame of one of their workshops in Budapest, Hungary. The date of the lunch-to-lunch workshop is 29-30 March 2007.

MINOS-EURONET is devoted to stimulating, encouraging and facilitating the participation of New Member States (NMS) and the Associated Candidate Countries (ACC) in the activities of IST. The network has a pan-European focus on one strategic objective in IST, namely micro- and nanosystems. The project is addressing the following objectives:

- Revealing and promoting the research competences, which are relevant for the development of micro-nanosystems at the European scale;
- Facilitating the participation of NMS and ACC organizations to EU programs and other activities in the field of micro-nanosystems;
- Performing extensive networking at the pan-European scale in the field of micro-nanosystems.

The **Info-day and Brokerage Event** will be devoted to:

1. Up-to-date information on FP7
2. Up-to-date information on the CLEAN project and the status of leakage aware design of nanometer CMOS circuits – The workshop is coupled with the Leakage Aware Design course of CLEAN IP
3. Brokerage of east-west research results, developments and applications – offers and demands on micro- and nano-systems – in order to establish potential partnership
4. Visiting laboratories

Who should attend?

- *Senior mangers* in organizations from *Automotive, Microelectronics, Defense, Biomedical* and other sectors with interests in micro-electronics
- *Professionals and technical experts* working in the area of Micro- and Nano- manufacturing

Participation and Registration
The participation in the brokerage event is ***free***.

Participants are invited to register on-line at www.ett.bme.hu/clean-minos or by email by contacting clean-minos@ett.bme.hu

Categories of participants expected:

- Eastern partners of the MINOS project
- Representatives and course lecturers of the CLEAN IP
- Western partners of the MINOS-EURONET project representing FP6 NoE's and IP's
- Representatives of the Hungarian research community and companies from the field of micro- and nano-systems, including nanometer structures, devices and circuits

For more information, please consult www.ett.bme.hu/clean-minos/.

Draft Agenda 1st day	**29 Mar, 2007**
Registration	10:30 – 12:30
Lunch	12:00 – 12:30
Parallel sessions: Leakage Aware Design course Visit to Labs of BME-ETT	12:30 – 19:30
Networking Dinner	20:00 - 22:00
Draft Agenda 2nd day	**30 Mar, 2007**
Information-day about FP7, Visit labs	08:30 – 12:00
National progress about first call of FP7 by Robert Dobay	08:30 – 09:00
Partner searching in Cordis by Hunor Santha	09:00 – 09:30
ICT Proposer of FP7 by Balint Balogh	09:30 – 10:00
Break	10:00 – 10:30
Presentation of Activities in the field of Micro and Nano structures, given by the meeting participants(cca 10min-10 PowerPoint slides each)	10.30 – 12.00
SME 1	
SME 2	
SME 3	
Lunch and Disperse	12:00 – 13:00

For the continuously updated program, please consult www.ett.bme.hu/clean-minos/.